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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/633,814 | 08/04/2003 | Hrvoje Jasa | Jasa 1-2-2 | 7482 |

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| EXAMINER | |
|---|---|
| KINKEAD, ARNOLD M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2817 | |

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/633,814 | JASA ET AL. | |
| | Examiner | Art Unit | |
| | Arnold M. Kinkead | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,14-20,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1,2,3,4,14-20,27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masenas et al(US 6,614,316) in view of Lebouleux(US 6,693,496).

The reference by Masenas et al discloses a phase locked loop(PLL) with phase detector(102), see figures 2 and 3, where the phase detector will generate up/down signals(303,304) based on a phase difference between a data signal(Fref) and a clcock signal(Fosc). That is, inherently the clock signal will be sampled by the data signal to allow for the generation of the error signal. A proportional charge pump(106)

generates a first voltage for a first time period; and an integral charge pump(108) generates a second voltage via (Cint) based upon the capacitance, and a truncated/masked inc/dec signals(see col.4, Lines 40-59). The second voltage is proportional to the current and capacitance, Vint=I/C; There is also a similar relationship for the Vproportional path. The stability being proportional to Vprop/Vint. A divide by N divider divides the output of the oscillator.

The reference does not show a resistor in the general proportional path block(106), and thus the Vprop = Iprop*R is not clear; however, the reference by Lebouleux is relied upon to show the resistive path(204) that is present in these PLL systems having both an integral and proportional path so as to represent the resistance of that path. Thus the Vprop=Iprop*R by virtue of this circuit arrangement. The reference by Masenas et al does not show a VCO but instead makes use of a current controlled oscillator. These two oscillators have been used in PLL loop applications and allow for an equivalent clock signal having a frequency. The reference by Lebouleux showing the VCO implementation and supports the use of such an equivalent clock output for sampling the data signal being inputted to the PLL. The method steps being inherent.

In light of the above it would have been obvious for one of ordinary skill in the art to have recognized that the proportional path, for conventional PLLs, do include resistance as highlighted by Lebouleux, in developing the error signal contribution. The use of a VCO instead of the ICO shown in Masenas et al provides more flexibility for the PLL designer, as both types may be used to produce the equivalent clock signal output with frequency determined by the error signal developed in the loop. The

reference by Lebouleux supporting such a VCO clock signal output. The function of the loop is still the same which is for clock generation based on the incoming data signal to the phase detector.

***Allowable Subject Matter***

4. Claims 5-13, and 21-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The examiner could not find fair suggestion for an LC type oscillator with setting..., a bang-bang PD, a MUX, a return/non-return to zero charge pump, etc...

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M. Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
Mar 31, 2005